EE 316: Advanced VLSI Devices
Lecture 0 – Administrative Details

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Administrative Details

- **Title:** Advanced VLSI Devices
- **Days/Times/Classroom:**
  - July 12-15, 14:00-16:00. Institute of Microelectronics Building, room 308 at Tsinghua University;
  - July 18-21, 8:30-10:30AM, classroom: Science Building 1, room 1131 at PKU;
  - July 25-28, 8:30-10:30AM, classroom: Institute of Microelectronics Building, room 308 at Tsinghua University;
  - August 1-4, 8:30-10:30AM, classroom: Science Building 1, room 1131 at PKU;
- **Course website:** TBD
Instructor and TA’s

Instructor: Prof. H.-S. Philip Wong

- Office: TBD
- Email: hspwong@stanford.edu

Teaching Assistant:

- 徐晓庆
Something About Your Professor

- [http://nano.stanford.edu](http://nano.stanford.edu)

H.-S. Philip Wong

**Professor of Electrical Engineering**

**Education:**

**Biography:**
Prof. Wong joined Stanford in September, 2004 after 16 years at IBM Research, T.J. Watson Research Center, Yorktown Heights, New York. While at IBM, he worked on CCD and CMOS image sensors, double-gate/multi-gate MOSFET, device simulations for advanced/novel MOSFET, strained silicon, wafer bonding, ultra-thin body SOI, extremely short gate FET, germanium MOSFET, carbon nanotube FET, and phase change memory. He held various positions from Research Staff Member to Manager, and Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM’s strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology.

His research interests are in nanoscale science and technology, semiconductor technology, solid state devices, and electronic imaging. He is interested in exploring new materials, novel fabrication techniques, and novel device concepts for future nanoelectronic systems. Novel devices often enable new concepts in circuit and system designs. His research also includes explorations into circuits and systems that are device-driven.
About Your TA – 徐晓庆
Course Objectives

- At the end of the course, you will be able to
  - Make projections about CMOS device scaling and how they affect circuit/system performance
  - Recognize the relevant device physics that underlies CMOS device design
  - Go to a conference or read a journal article about CMOS devices and use the knowledge obtained in this course to understand the papers
  - Design a state-of-the-art MOSFET, project its performance
    - Use device modeling (TCAD) tools and interpret results from device modeling
- Develop an intuitive feel in addition to solving equations
Homework and Grading Policy

- **Grading:**
  - Exam: 50%
    - Date to be determined
  - Homework: 50%

- **Homework:**
  - About twice a week
  - Some homework are literature reading assignments with specific questions aimed at probing your understanding of the material
    - Develop skills in reading current literature with focused reading
    - Cover topics that we do not have time to cover in the lectures
    - Same skills required for PhD research or R&D job in companies
Late Homework Policy

- Submit by due date, class time – full credit
- Submit by next day, class time – 25% off
- Submit by day after next, class time – 50% off
- After that, no credit
- Solutions will be posted soon after the homework is collected
Questions?
Textbook

Textbook:

  - ISBN # 0-521-55959-6 (paperback, 1st edition)
  - Roughly, I will cover Chapters 1 – 5 and 10

Course notes:

- Available on-line (course website), posted before the lecture
  - Notes are organized in “Lectures” (0 – 10) around major topics
  - Number in the lower bottom are “x-y”, where x=Lecture #, y=slide #
  - Plenty of references at most slides for further study – please read them
- Course notes sources: courtesy of Prof. S. Simon Wong, Prof. Krishna Saraswat, Prof. Yuan Taur (UCSD), Dr. Tak H. Ning (IBM Research)
References

Device physics:


Conference proceedings:

- IEEE International Electron Devices Meeting (IEDM) – access: IEEE Xplore
- Symposium of VLSI Technology – access: IEEE Xplore
- IEEE journals: http://ieeexplore.ieee.org/Xplore/dynhome.jsp?tag=1
Assumptions and Background

- EE 216
- Muller & Kamins book
- Chapter 2 (except 2.4, 2.5) of Taur & Ning book (2nd edition)
- Undergraduate level knowledge of device fabrication
- Undergraduate level knowledge of CMOS circuits
Topics To Be Covered (1 of 2)

- Overview of the semiconductor industry
- MOSFET – MOS capacitor, MOSFET long channel behavior
- Si MOSFET device scaling, non-scaling factors, reading the ITRS
- Short-channel MOSFET
- Device modeling
  - TCAD tools, fundamentals of numerical device simulation, interpretation of device simulation results and tricks of the trade
  - TA sessions for Sentaurus modeling tool prior to lecture
- MOSFET electrostatics
  - Channel length, scale length theory, minimum channel length
  - PDSOI, FDSOI, double-gate, FinFET, multi-gate FET
  - Threshold voltage, quantum effects
  - Non-uniform channel doping, halo, super-halo
- MOSFET electrodynamics
  - Carrier mobility, velocity saturation, scattering theory, ballistic transport
  - Strain effects
Topics To Be Covered (2 of 2)

- **High field effects**
  - Impact ionization and breakdown, band-to-band tunneling, tunneling into gate dielectrics, hot carriers, dielectric degradation mechanisms

- **CMOS performance factors**
  - CMOS circuit elements, propagation delay, delay metrics, power dissipation
  - Interconnect R and C, interconnect scaling
  - Parasitic elements, device pitch scaling
  - Device design tradeoff
Questions?